BLL2752

40V, 15A CV and Dual CC Step-Down DC/DC Controller

DESCRIPTION

BLL2752 has an optimum input voltage, step-down controller that operates in either CV (Constant output Voltage) mode or CC (Constant output Current) mode. The maximum input voltage is up to 40V and the operation input voltage from 8.5V to 32V.

External compensation is not needed. It consists of inside line compensation function with 150mV at V_{IN}=12V, I_{OUT}=15A.

In conclusion, BLL2752 is a full function and high performance, high reliability buck DC-DC converter.

FEATURES

- External high-side and low-side MOSFET
- Max output current: 15A
- Constant output voltage: 5.05V
- Excellent constant current accurate: ±7%
- Constant voltage accurate: ±2%
- No external compensation needed
- Jitter function
- Efficiency: up to 96%
- Line compensation: Typ. 150mV@V_{IN}=12V
- Short circuit protection
- Over voltage protection
- Thermal shutdown protection
- Under voltage lock-out
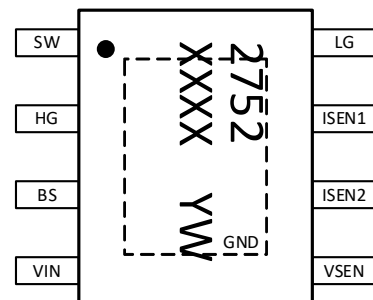- Available in ESOP-8 package
- ESD HBM >5KV

APPLICATIONS

- Car DVD
- Black box
- Car charger
- Industry application

ORDERING INFORMATION

Part No.	Package	Tape&Reel
BLL2752CS8TR	ESOP-8	4000/Reel

PIN OUT & MARKING

ESOP-8

2752: Product Code
XXXX: Lot No.
YW: Date code (Year & Week)

TYPICAL APPLICATION

Dual Channel Application

Single Channel Application
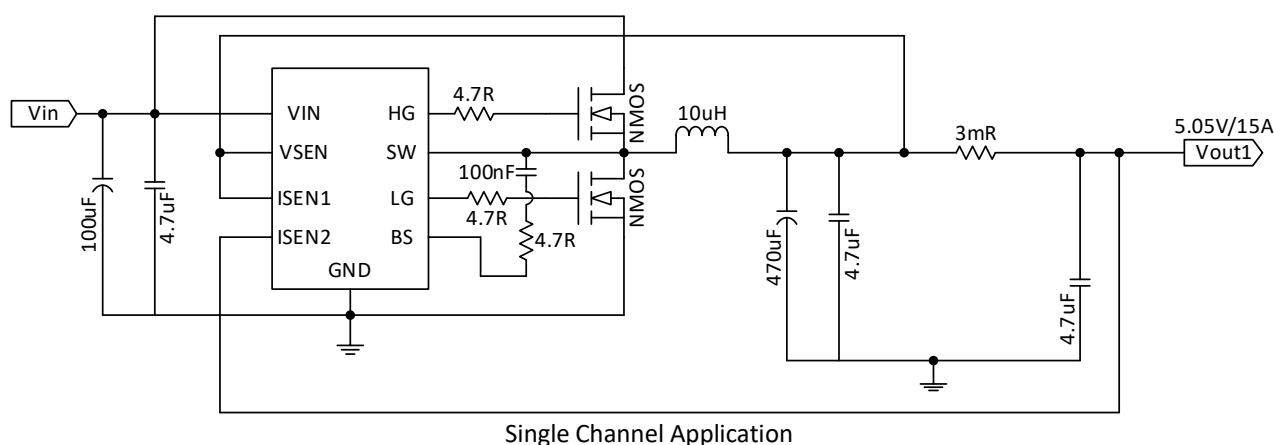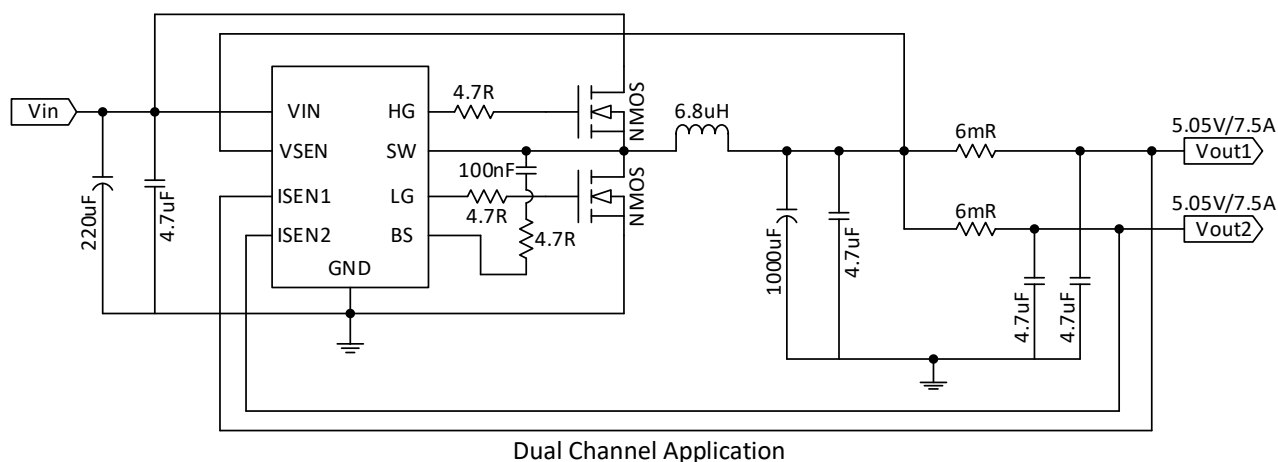
PIN DESCRIPTION

Pin #	Name	Description
1	SW	Power switching output connect to external inductor.
2	HG	Driver of high side NMOS, connect to the gate of NMOS.
3	BS	Power to the internal high-side MOSFET gate driver. Connect a 100nF capacitor from BS to SW.
4	VIN	Power supply input. Place a 4.7μF ceramic capacitor between VIN and GND as close as possible.
5	VSEN	Sense of output voltage.
6	ISEN2	Current sense input2.
7	ISEN1	Current sense input1.
8	LG	Driver of low side NMOS, Connect to the gate of NMOS.
9	GND	Ground.

ABSOLUTE MAXIMUM RATING

Parameter		Value
VIN to GND		-0.3V to 42V
SW to GND		-0.3V to VIN
BS to GND		(V_{SW}-0.3V) to (V_{SW}+6V)
ISEN1, ISEN2, HG, LG, VSEN to GND		-0.3V to 6V
Max operating junction temperature (T_J)		125°C
Ambient temperature (T_A)		-40°C to 85°C
Package thermal resistance (θ_{JC})	ESOP-8	10°C/W
Storage temperature (T_S)		-40°C to 150°C
Lead temperature & time		260°C, 10s
ESD (HBM)		>5000V

Note: *Exceed these limits to damage to the device.*

*Exposure to absolute maximum rating conditions may affect device reliability.*

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_A=25°C, unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input voltage		8.5	-	40	V
$V_{OVP-VIN}$	Input OVP threshold		30	32	34	V
V_{UVLO}	UVLO voltage		-	8	9	V
	UVLO hysteresis		-	1	-	V
I_{CCQ}	Quiescent current	V_{SENSE}=5.8V	-	1.6	2.5	mA
I_{SB}	Standby current	No load, V_{IN}>8.5V	-	1.6		mA
V_{OUT}	Output voltage	I_{OUT}=1A	4.95	5.05	5.15	V
V_{SEN}	Output OVP detect voltage	Internal defined	-	6.2	-	V
F_{SW}	Switching frequency	I_{OUT}=1A	-	130	-	KHz
Reference of $V_{SEN}-I_{SEN}$	Reference voltage of constant current	2.4V<V_{OUT}<4.5V	55.8	60	64.2	mV
	Minimum on-time		-	120	-	ns
	Line compensation	V_{IN}=12V, I_{OUT}=15A	-	150	-	mV
I_{Limit}	Secondary cycle-by-cycle current limit	Minimum duty cycle, no CC	-	8.5	-	A
$IMAX_{SINK}$	DRV max current		-	-	1.2	A
$IMAX_{PULL}$			-	-	0.7	A
T_{SD}	Thermal shutdown temp		-	155	-	°C
T_{SH}	Thermal shutdown hysteresis		-	30	-	°C

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs. Iout

Vin=12V
Vin=24V
Vin=31V
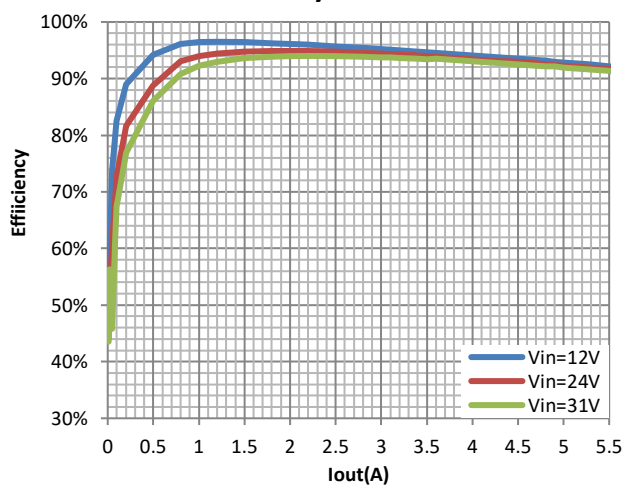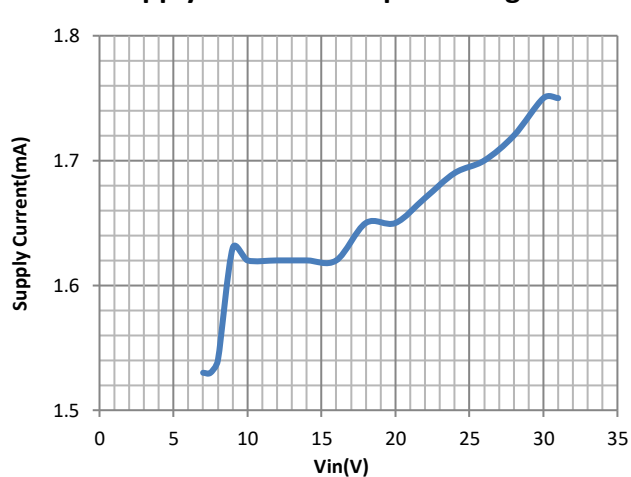
Iin vs. Temp
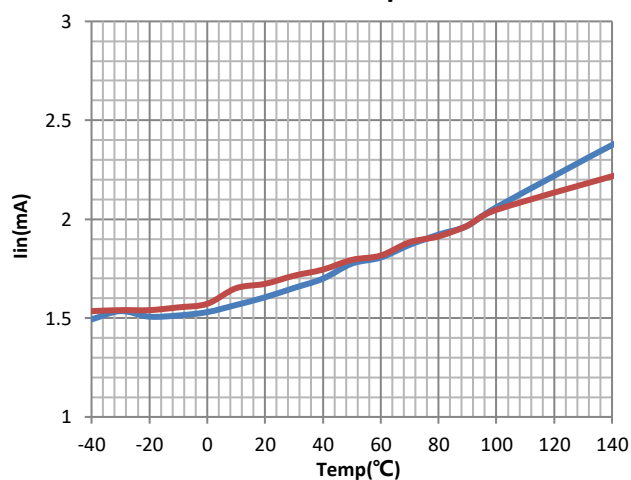
Switch Frequency vs. Input Voltage
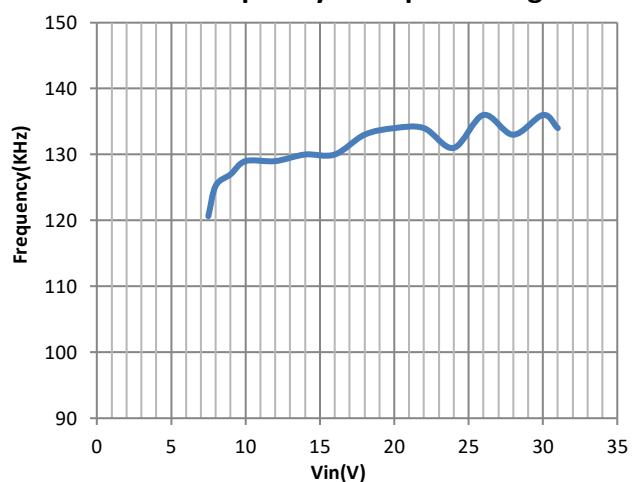
Supply Current vs. Input Voltage

Short Circuit
Vin=12V, Freq=2Hz

500ms
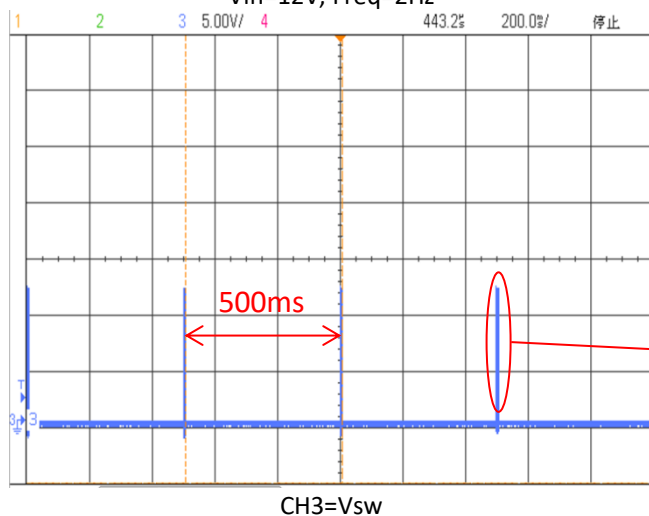
CH3=Vsw

Short Circuit
Vin=12V, Freq=34KHz

CH3=Vsw

BLL2752
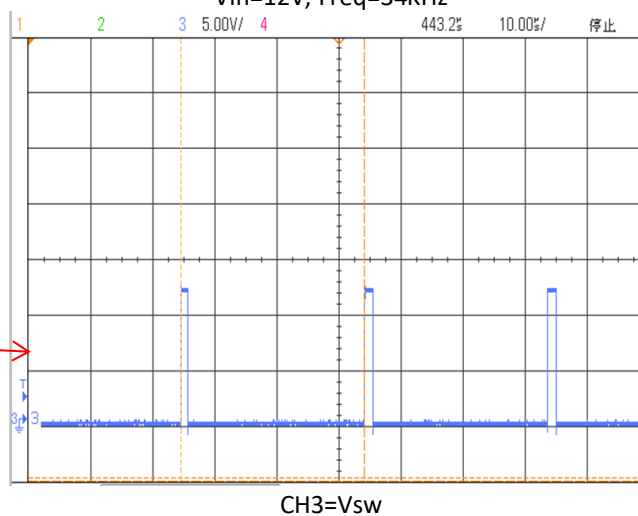
Power On
Vin=12V, Vout=5.05V, Iout=5.5A
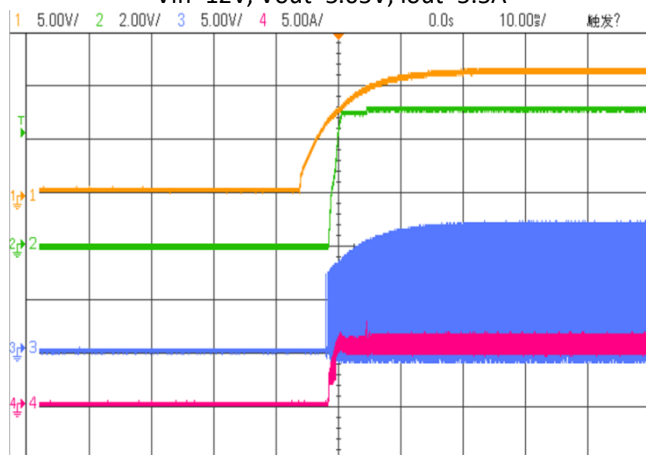
CH1=Vin, CH2=Vout, CH3=Vsw, CH4=Isw

Power Off
Vin=12V, Vout=5.05V, Iout=5.5A

CH1=Vin, CH2=Vout, CH3=Vsw, CH4=Isw
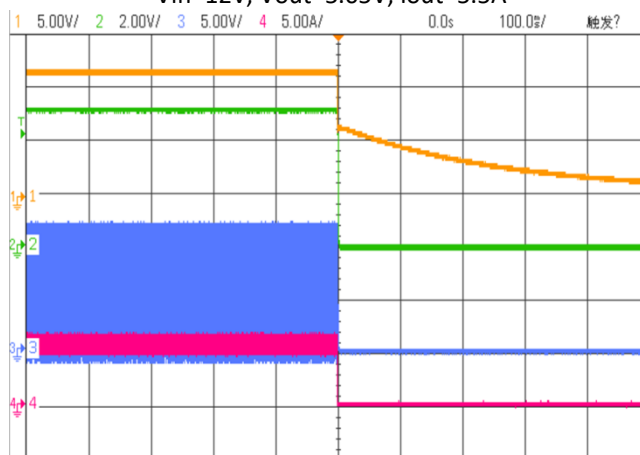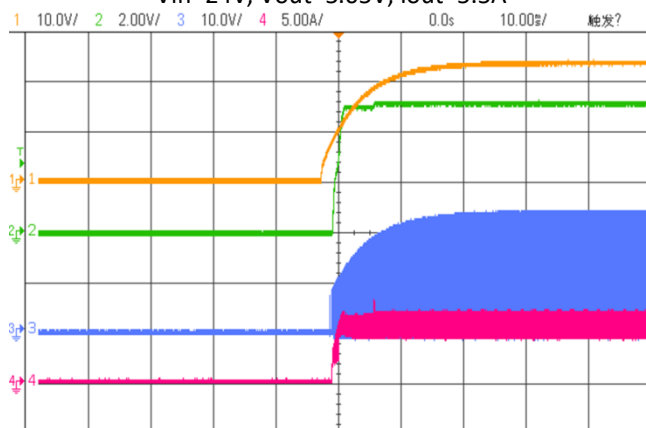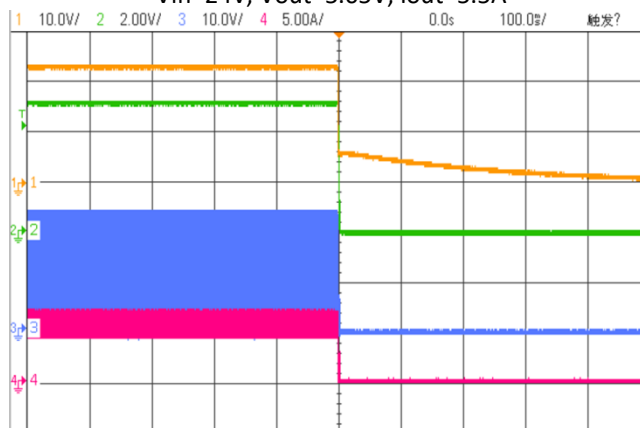
Power On
Vin=24V, Vout=5.05V, Iout=5.5A

CH1=Vin, CH2=Vout, CH3=Vsw, CH4=Isw
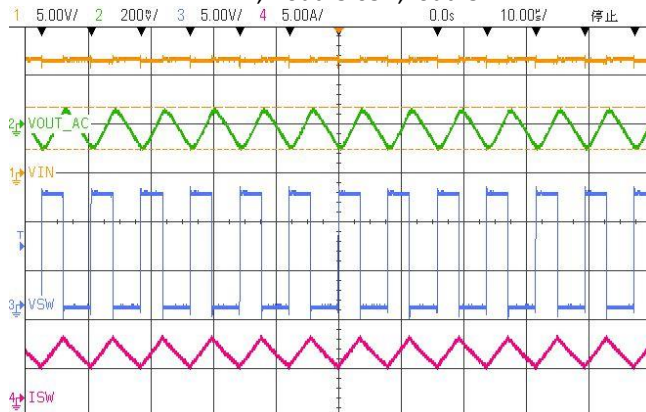
Power Off
Vin=24V, Vout=5.05V, Iout=5.5A

CH1=Vin, CH2=Vout, CH3=Vsw, CH4=Isw
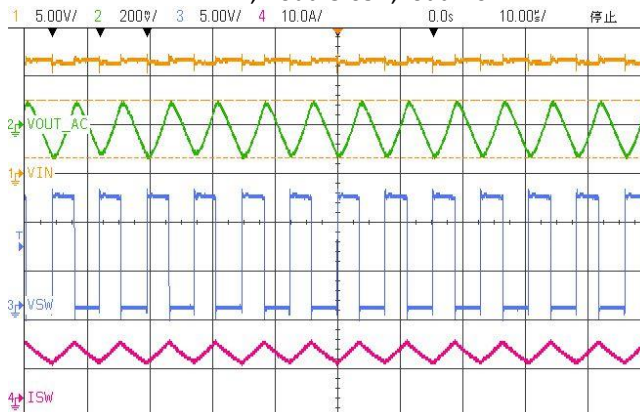
Output Voltage Ripple
Vin=12V, Vout=5.05V, Iout=5A

CH1=Vin, CH2=Vout_ripple, CH3=Vsw, CH4=Isw

Output Voltage Ripple
Vin=12V, Vout=5.05V, Iout=10A

CH1=Vin, CH2=Vout_ripple, CH3=Vsw, CH4=Isw

DETAILED DESCRIPTION

Input Under Voltage Protection

BLL2752 provides an input voltage up to 40V and operates from an input voltage range of 8.5V to 32V. If VIN drops below 7V, the UVLO circuit inhibits switching. Once VIN rises above 8V, the UVLO clears, and the soft-start sequence activates.

Input Over Voltage Protection

If VIN rises above 32V, the OVP circuit inhibits switching. BLL2752 will not be damaged until the voltage exceeds 40V. Once VIN drops below 29V, the OVP clears, and the soft-start sequence activates.

Soft-start

BLL2752 has an internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lock-out (UVLO), shutdown mode, or restarts following a thermal-overload event, the soft-start circuitry slowly ramps up current available after 300us.

Constant Voltage Output

BLL2752 presets the output voltage to 5.05V.

Output Over Voltage Protection

Once VSEN rises above 6.2V, BLL2752 shuts down to avoid damage caused by abnormal use of electrical equipment.

Constant Current Output

BLL2752 senses the current by sampling the voltage difference between VSEN and ISEN, and adjusts the output current to the default value by the loop.

$$I_{OUT1} = \frac{60mV}{R_{ISEN1}}, \quad I_{OUT2} = \frac{60mV}{R_{ISEN2}}$$

Constant current operates normally when VSEN is higher than 2V. When VSEN is below 1.9V causing by overload, BLL2752 will enter short circuit protection mode.

Short Circuit Protection

When ISEN1 and ISEN2 drop below 1.9V since too heavy load, BLL2752 will enter short circuit protection function, and the system will enter hiccup mode, and frequency will drop to 34KHz per cycle and stop switching for 500ms.

Line Compensation

When the output current rises from 0mA to full load, the output voltage will be increased by 150mV (typical) for line compensation.

Thermal Shutdown

The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 155°C), the controller shuts off. This is non-latch protection. There is about 30°C hysteresis. Once the junction temperature drops around 125°C, soft start is initiated.

LAYOUT GUIDE

1. PCB trace defined as SW node, which connects to source of switching MOSFET, drain of rectifying MOSFET and high-voltage side of the inductor, should be as short and wide as possible.
2. Switching nodes such as SW, HG or LG nodes to avoid coupling.
3. Cin input bypass capacitor should be placed to the VIN pin as close as possible.
4. Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use a 0.65mm (25mils) or wider trace.
5. Gather the ground terminals of the VIN capacitor(s), VOUT capacitor(s), and the source of the low-side MOSFETs as close as possible.
6. VSEN&ISEN connect to R_{ISEN} directly as short as possible.

BLL2752

PACKAGE OUTLINE

Package	ESOP-8	Devices per reel	4000pcs

Package dimension:

SECTION A-A

BASE METAL

Dimensional References							unit:mm
Ref.	MIN	NOM	MAX	Ref.	MIN	NOM	MAX
A	1.35	1.55	1.75	E1	5.8	6.0	6.2
A1	0.10	0.15	0.25	L	0.45	0.60	0.80
A2	1.25	1.40	1.65	L1		1.04 REF	
A3	0.5	0.6	0.7	L2		0.25 BSC	
b	0.38	/	0.51	R	0.07	/	/
b1	0.37	0.42	0.47	R1	0.07	/	/
c	0.17	/	0.25	Ø	0°	/	8°
c1	0.17	0.20	0.23	Ø1	15°	17°	19°
D	4.8	4.9	5.0	Ø2	11°	13°	15°
d		1.27 BSC		Ø3	15°	17°	19°
E	3.8	3.9	4.0	Ø4	11°	13°	15°
D1	3.2	3.3	3.4				
E2	2.3	2.4	2.5				
aaa		0.10		bbb		0.10	
ccc		0.10		ddd		0.25	

Note:
a. All dimension are in millimeter.
b. Exposed metallized leads are Cu with surface finish protection.
c. E dose not include mold protrusion(flash). Max flash is 0.25mm per side.
d. D dose not include mold protrusion(flash). Max flash is 0.25mm per side.
e. b dose not include dam bar protrusion. Allowable dam bar protrusion in maximum material condition. Dam bar cannot be located on the lower radius or the foot. Minimum space between dam bar protrusion and adjacent lead to be 0.07 mm.
f. Plating material: 100% (Matte) Sn.
g. General appearance spec. should be based on final visual inspection spec.